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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/535,553
Filing Date: May 18, 2005
Appellant(s): DONALDSON ET AL.

Kenneth D. Springer
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 6/19/07 appealing from the Office action mailed 1/19/07.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

EP 1065600 A2	Buhring	01-2001
6710626	Buhring	03-2004
20020154524	Yamanaka et al.	10-2002
6493275	Tomita	12-2002
6204649	Roman	03-2001

6087857 Wang 07-2000

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-4, 6-12, 14-16, and 18-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Buhring (EP 1065600), Applicant's submitted IDS.

As to claim 1, Burhring's figure shows a device comprising: a floating bus (CHN_H, CHN_L); power and data system (6-8, 11, 18, 19) for driving the floating bus, the power and data system comprising a charge pump circuit; and at least one switch control circuit (9, 10, 14, 15, 20) coupled to the floating bus and the power and data system for facilitating charging of the floating bus and for controlling electromagnetic emission from the device (it is inherent that circuit (9, 10, 14, 15, 20) controls some of or little the EME of the circuit).

As to claim 2, the figure shows that the at least one switch control circuit comprises a first switch control circuit and a second switch control circuit, the first switch control circuit comprising at least one P type transistor circuit (9), and the second switch control circuit comprising at least one N type transistor circuit (10) and wherein the first switch control circuit and the second switch control circuit comprise complementary circuits.

As to claim 3, the figure shows that the first switch control circuit is electrically connected to a first bus node of the floating bus and the second switch control circuit is electrically connected to a second bus node of the floating bus.

As to claim 4, the figure shows that the charge pump circuit comprises an integrated circuit employing at least one transistor and diode pair.

As to claim 6, the figure shows that the floating bus comprises a balanced bus system having a high side bus node and a low side bus node, and wherein the at least one switch control circuit comprises a first switch control circuit and a first diode connected to the high side bus node and a second switch control circuit and a second diode connected to the low side bus node.

As to claim 7, the figure shows that the first switch control circuit and the second switch control circuit are driven by a reference circuit (circuit, not shown, that providing supply voltages to circuit 14 and 15), the reference circuit generating a first reference signal for the first switch control circuit and a second reference signal for the second switch control circuit.

As to claim 8, the figure shows that when a voltage across a first terminal and a second terminal of the first switch control circuit is greater than a threshold value (a threshold value may be any value), output current from the first switch control circuit is constant at a value dependent on the first reference signal (clearly the output current is dependent on the power supply voltage of 14 and 15), and when voltage across a first terminal and a second terminal of the second switch control circuit is greater than the threshold value, output from the second switch control circuit is constant at a value dependent on the second reference signal.

As to claim 9, the figure shows that the at least one switch control circuit controls electromagnetic emission from the device by constraining the slew rate on the floating bus.

As to claim 10, the figure shows a circuit comprising: a first switch control circuit (9, 20, 14) for electrical coupling to a high side bus node of a floating bus, and a second switch control circuit (10, 15) for electrical coupling to a low side bus node of the floating bus, wherein the first switch control circuit and the second control circuit comprise complementary circuits for

controlling charging of the floating bus by a power and data system; and a reference circuit for generating a first reference signal for the first switch control circuit and a second reference signal for the second switch control circuit, wherein the first reference signal and the second reference signal are employed by the first switch control circuit and the second switch control circuit, respectively, for controlling electromagnetic emissions from the floating bus by constraining a slew rate on the floating bus.

As to claim 11, the figure shows that the power and data system comprises a charge pump circuit, the charge pump circuit comprising an integrated circuit.

As to claim 12, the figure shows that the first switch control circuit comprises a P type transistor circuit, and the second switch control circuit comprises a complementary N type transistor circuit.

As to claim 14, the figure shows a method comprising: tailoring a transfer characteristic of a first switch control circuit (9, 14, 20) to be electrically coupled to a high side bus node of a floating bus, and tailoring a transfer characteristic of a second switch control circuit (10, 15) to be electrically coupled to a low side bus node of the floating bus, wherein the first switch control circuit and the second switch control circuit comprise complementary control circuits for controlling charging of the floating bus by a power and data system; and generating, when in use, a first reference signal (power supply of 14) for the first switch control circuit and a second reference signal (power supply of 15) for the second switch control circuit, wherein the first reference signal and the second reference signal are employed by the first switch control circuit and the second switch control circuit, respectively, for controlling electromagnetic emission from the floating bus by constraining a slew rate on the floating bus.

As to claim 15, the figure shows that the power and data system comprises a charge pump circuit, the charge pump circuit comprising an integrated circuit.

As to claim 16, the figure shows the step of integrating the first switch control circuit and the second switch control circuit on the integrated circuit with the charge pump circuit.

Claim 18 recites similar limitations of claim 10. Therefore, it is rejected for the same reasons.

As to claim 19, the figure shows that the switch control circuit includes: a switch (9) selectively connecting the floating bus to the power and data system; and slew rate adjusting means (20) for adjusting a slew rate of a voltage on the floating bus when the switch connects floating bus to the power and data system.

As to claim 20, the figure shows that the slew rate adjusting means is responsive to a reference current (current generated by 15), wherein when the reference current has a first value (when 20 is off), the slew rate adjusting means adjusts the slew rate of the floating bus to be a first slew rate, and wherein when the reference current has a second value (when 20 is ON), the slew rate adjusting means adjusts the slew rate of the floating bus to be a second slew rate greater than the first slew rate.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 5, 13 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Buhring (EP 1065600) in view of Yamanaka (US 20020154524).

Buhring's figure shows all limitations of the claims except for that "the at least one switch control circuit is operable in at least a low speed mode and a high speed mode, with mode of the at least one switch control circuit being dependent upon a desired floating bus charging speed".

However, Yamanaka's figures 2-5 shows charge pump circuit having voltage detecting circuit (i.e. 2-11 and 22 in figure 2) for controlling the speed of the switches in order to reducing rush current. Therefore, it would have been obvious to one having ordinary skill in the art to employ Yamanaka teaching to control the switches' speeches of Buhring in order to reduce rush current.

(10) Response to Argument

Appellant argues that Buhring does not disclose the switch control circuit that is used "for controlling electromagnetic emission from the device", pages 6-8. The Examiner respectfully disagrees. It is notoriously well known that switching transistors generate alternative currents in response to alternative input signals. It is also known that alternative currents create electromagnetic field, thereby generate electromagnetic interface emission. The teaching of switching transistors generate electromagnetic interface emission is disclosed in Tomita (USP 6493275), col. 1, lines 10-26 and lines 58-60, and in Roman (USP 6204649), col. 1, lines 35-41. Appellant further admits that Buhring switches generate electromagnetic emission (page 6, lines 10-14 under ARGUMENTS). Buhring's switch transistors 9, 10 and 20 are turned on/off by frequencies generated by circuits 14 and 15. Thus, the electromagnetic emission is generated based on the switching frequencies of the transistors. Furthermore, Buhring corresponds to U.S. Patent 6710626, which teaches in col. 1, lines 31-35, that the circuit is for reducing electromagnetic radiation when switching the states. Therefore, the electromagnetic emission is controlled by the switching frequencies of the transistors 9, 10 and 20.

In response to the argument regarding the rejection of claim 7, pages 8-9, any voltage can be considered as a signal, AC voltage signal or DC voltage signal. Power supply voltage can also be considered as a signal or a reference signal. Evidence that teaches power supply

is considered as a signal is disclosed in Wang (USP 6087857), col. 1, line 22, which shows that Vdd is a supply voltage signal.

In response to the argument regarding the rejection of claim 8, pages 9-10, with broadest reasonable interpretation, any value can be considered as the claimed threshold value, i.e. zero (0) which can be considered as the claimed threshold value. Clearly, voltage across the first and second terminals of the first switch control circuit is greater than zero.

Appellant further argues that the output current is not dependent on the power supply voltage of 14 and 15. The Examiner respectfully disagrees. It is inherent that transistor's gate voltage determines current through its drain-source. The output voltages of circuits 14 and 15 are the gate voltages of transistors 9, 10 and 20. Clearly, the output voltages of 14 and 15 are determined by the supply voltages of 14 and 15, i.e. output voltages of 14 and 15 would not be equal to 5 volts if the supply voltages of 14 and 15 were less than 5 volts, or the output voltages maybe higher than 5 volts if the supply voltages were 10, 30 or 30 volts. Therefore, the currents generated by transistors 9, 10 and 20 are dependent upon the power supply voltages of 14 and 15.

In response to the argument regarding the rejection of claim 9, pages 10-11, clearly current generated by circuit comprising transistors 9 and 20 when both transistors are on is more than current generated by the circuit when only one of the transistors is on. The generated current determines the speed of the circuit, thus determines the slew rate at the circuit's output or on the bus.

Appellant cites col. 4, lines 5, col. 5, line 8 of Buhring corresponds to US Pantent 6710626 to reason that transistors 9 and 20 would not be on at the same time. The Examiner respectfully disagrees. Buhring corresponds to US Patent 6710626's col. 5, lines 3-5, teaches that MOSFET 20 in normal cases "can generally not be turned on". It is noted that "generally"

does not mean "always". Furthermore, col. 5, lines 9-13, teaches that transistor 9 can be turned on and transistor 20 can be turned to a limit extent in normal cases". Therefore, transistors 9 and 29 would be turned on at the same time to a limit extent in normal cases.

In response to the arguments regarding the rejection of claims 10-12, 14-16 and 18-20, Appellant addresses the same arguments regarding the rejections of claims 1, 7, 9. Therefore, the same responses are applied.

In response to the argument regarding to the rejection of claims 5, 13 and 17, pages 14-15, Buhring's figure and Yamanaka et al.'s figures 2-5 are both charge pump circuits. Yamanaka uses voltage detection circuit 2-11 and 22 in figure 2 to adjust the speed of the switch control signals dependent upon the output level in order to maintain a desired output voltage level. Therefore, it would have been obvious to one having ordinary skill in the art to employ Yamanaka's teaching to control Buhring's transistors' switching speeds in order to provide a precise output level. Thus, the newly added voltage detection must be coupled to Buhring's output, which is the floating bus, to detect the output voltage. It is inherent that output current is proportional to the output voltage (V = I*R). Thus, the charging speed (output current) is detected by the newly added voltage detector. Therefore, the modified a Buhring's figure shows the claimed limitation: "the at least one switch control circuit (switches 9, 10 and 20) is operable in at least a low speed mode and a high speed mode (adjusted by the detector), with mode of the at least one switch control circuit being dependent upon a desired floating bus charging speed".

Appellant further argues that the Examiner fails to mention the features of claim 13 wherein the node of the mode of the first switch control circuit and the second switch control circuit are determined by the first and second reference signals generate by the reference circuit in response to an input control signal. The Examiner respectfully disagrees. Yamanaka et al.

controls supply voltage level of reference signal (output of 6 and 7, figures 2 and 3) in order to control the switching speeds. Therefore, the newly added voltage detector must control the supply voltage levels of Buhring's 14 and 15 in order to control the circuit switching speeds. Thus, the modified Buhring's figure shows the mode of the first switch control circuit and the second switch control circuit are determined by the fist and second reference signals (power supplies of 14 and 15) generate by the reference circuit in response to an input control signal (output of the newly added detector).

A similar response is applied to the argument regarding to the rejection of claim 17 since similar argument has been address.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

(12) Conclusion

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

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